

40V 1.2A Step-Down Dimmable LED Driver

additional information on the flexible external PWM dimming method, please refer to the “Selecting Dimming Control Mode” section.

System Soft Start

The voltage on the EN/DIM pin is the inductor current reference. An external capacitor from the EN/DIM pin to ground provides a soft-start delay.

Dimming Control

BM4115 provides two dimming methods: PWM dimming and DC analog dimming.

To use PWM dimming, apply a square wave to the EN/DIM pin. To use analog dimming, apply a 0.3V-to-2.5V DC voltage to this pin.

Application Information

Setting the LED Current

The LED current is set by the current-setting resistor between the IN and RS pins, where:

$$R_{SET} = \frac{100mV}{I_{LED}}$$

For $R_{SET}=0.2\Omega$, the LED current is set to 500mA

Selecting the Inductor

Lower value of the inductor results in higher switching frequencies, leading to larger switch loss. For most applications, select a switching frequency between 200kHz and 600kHz. Estimate the inductor value based on the desired switching frequency, where:

$$L = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{0.4 \times I_{LED} \times f_{SW}}$$

For higher efficiency, use inductors with low DC resistance.

Selecting the Diode

The output diode supplies current flowing path to the inductor when the internal MOSFET is off. To reduce losses due to the diode forward voltage and recovery time, use a Schottky diode. Select a diode rated with a reverse voltage greater than the input voltage. The average current rating must exceed the maximum expected load current, and the peak current rating must exceed the peak inductor current.

Selecting Soft-Start Capacitor

The delay time with the soft-start capacitor can be estimated by 0.2ms/nF. In PWM dimming, select a $C < 2.2nF$ to eliminate its effect on the average LED current.

Selecting Dimming Control Mode

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BM4115 provides two dimming methods: DC analog dimming and PWM dimming.

1. DC analog dimming mode

Apply a 0.3V-to-2.5V DC voltage to the EN/DIM pin. The voltage from 0.3V to 2.5V changes the inductor current reference directly and linearly controls the inductor current range from 25% to 100% (see Figure 2).

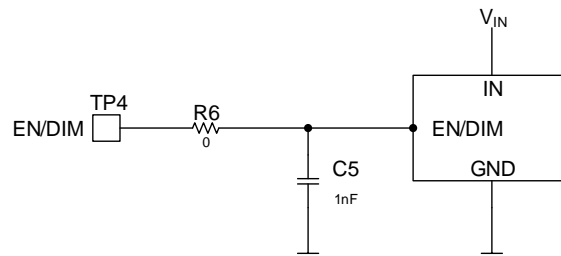


Figure 2: Analog Dimming External Circuit

The average output current is given by:

$$I_{OUT} = \frac{0.1 \times V_{DIM}}{2.5 \times R_S}$$

$$0.5V < V_{DIM} < 2.5V$$

2. PWM dimming mode

Apply a 100Hz-to-2kHz square waveform to the EN/DIM pin. The average LED current is proportional to the PWM duty cycle. Add an NPN transistor on/off circuit to separate the PWM signal from the current reference (see Figure 3) because this pin is pulled up by the 1.25V internal source as the inductor current reference. The minimum PWM amplitude is 1.5V.

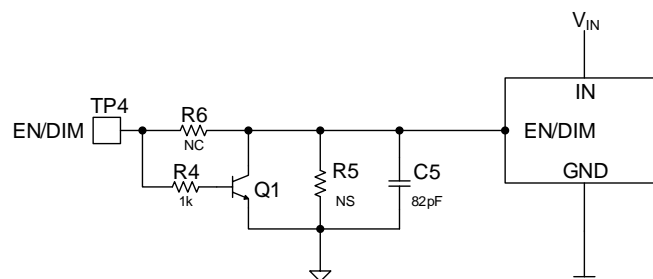
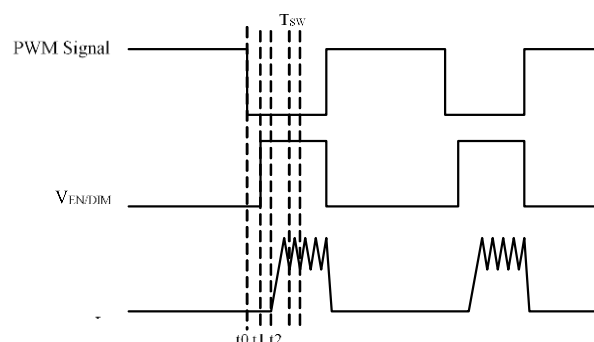


Figure 3: PWM Dimming External Circuit



t0-t1: Delay time caused by transistor turning-off. t1 is about 1us-2us t1-t2: Delay time caused by signal transmission (less than 1us).

T_{sw}: one switching period

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The average LED current is proportional to duty cycle of PWM signal. For good PWM dimming linearity, inductor current has to achieve the peak threshold during PWM on time. The minimum PWM duty cycle can be estimated as below:

$$\frac{D_{MIN}}{f_{PWM}} = t1 + t2 + 4 \times D \times T_{SW}$$

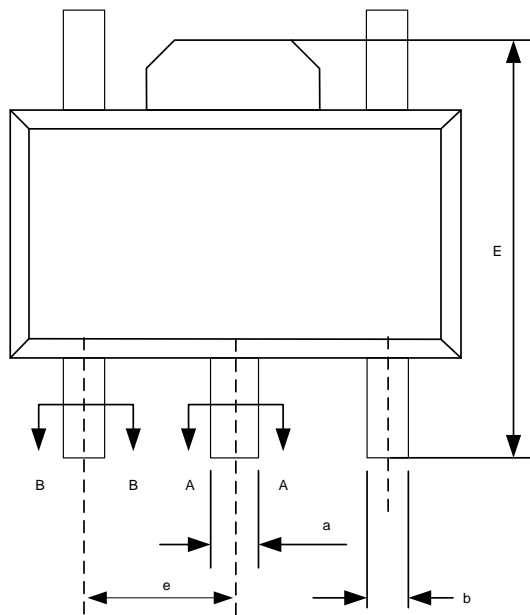
Circuit Layout Consideration

Pay careful attention to the PCB board layout and components placement. R_{SENSE} should be placed close to the IN pin and RS pin to minimize set current error. The input loop including the input capacitor, Schottky diode, and internal MOSFET should be as short as possible.

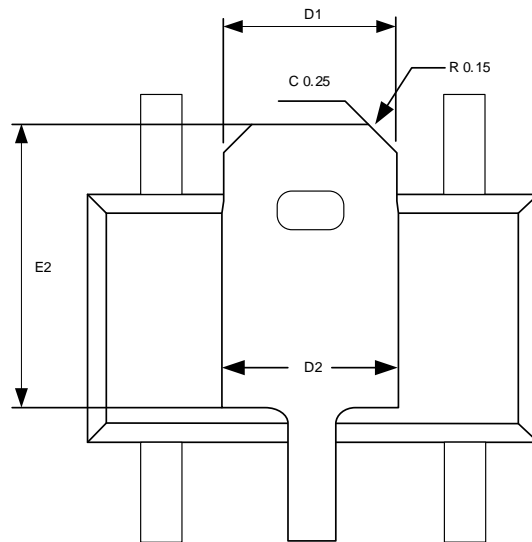
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Package Description

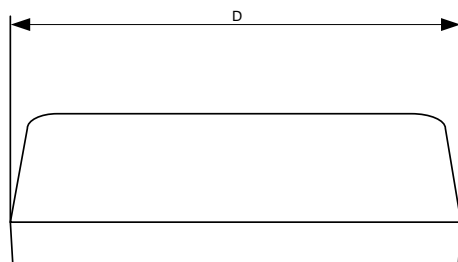
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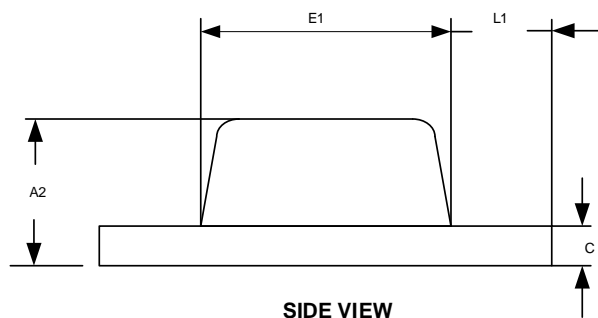
TOP VIEW



BOTTOM VIEW



FRONT VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A2	1.40	1.50	1.60
b	0.38	-	0.46
a	0.46	-	0.56
D	4.40	4.50	4.60
E	4.00	4.20	4.40
E1	2.40	2.50	2.60
e	1.50BSC		
L1	0.80	1.00	1.20

Size(mm) L/F Size(mil)	D1	D2	E2
	85×70	1.70REF	1.75REF

- NOTE:
- CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
 - PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
 - PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
 - LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
 - DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
 - DRAWING IS NOT TO SCALE.