

100V N-Channel Enhancement Mode MOSFET

■ DESCRIPTION

The 15N10 is N channel enhancement mode power effect transistor which is produced using high cell density advanced trench technology.

The high density process is especially able to minimize on-state resistance. These devices are especially suited for low voltage application power management DC-DC converters.

■ FEATURE

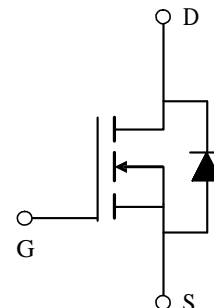
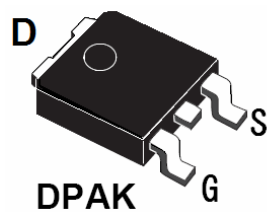
- ◆ 100V/15 A, $R_{DS(ON)}=80.0m\Omega$ (typ.)@VGS=10V
- ◆ 100V/8A, $R_{DS(ON)}=115m\Omega$ (typ.)@VGS= 4.5V
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ Full RoHS compliance
- ◆ SOP8 ,SOT23 andTO252 package design
- ◆ 100% UIS Tested
- ◆ 100% Rg tested

■ APPLICATIONS

- ◆ Power Management
- ◆ DC/DC Converter
- ◆ Load Switch

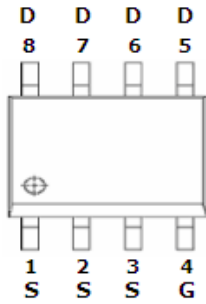
■ PIN CONFIGURATION

TO-252



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SOP-8



SOT-23



Common Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)				
V_{DSS}	Drain-Source Voltage	100	V	
V_{GSS}	Gate-Source Voltage	± 20		
T_J	Maximum Junction Temperature	175	$^\circ\text{C}$	
T_{STG}	Storage Temperature Range	-55 to 175	$^\circ\text{C}$	
I_S	Diode Continuous Forward Current	5	A	
I_{DP}	300 μs Pulse Drain Current Tested	$T_C=25^\circ\text{C}$	64	A
		$T_C=100^\circ\text{C}$	44	
I_D	Continuous Drain Current	$T_C=25^\circ\text{C}$	15	A
		$T_C=100^\circ\text{C}$	11	
P_D	Maximum Power Dissipation	$T_C=25^\circ\text{C}$	60	W
		$T_C=100^\circ\text{C}$	30	
$R_{\theta JC}$	Thermal Resistance-Junction to Case	2.5	$^\circ\text{C}/\text{W}$	
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	50	$^\circ\text{C}/\text{W}$	
E_{AS}	Avalanche Energy, Single Pulsed (L=0.3mH)	30	mJ	

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■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ Unless otherwise noted)

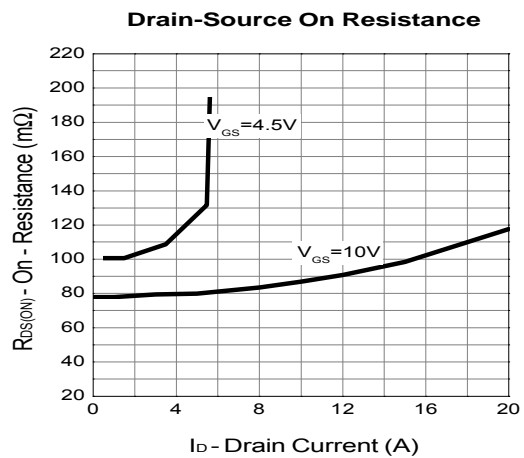
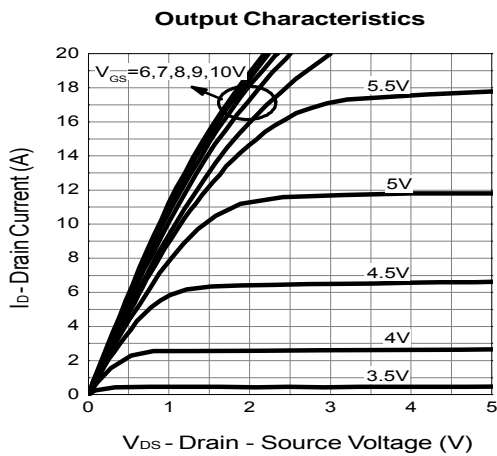
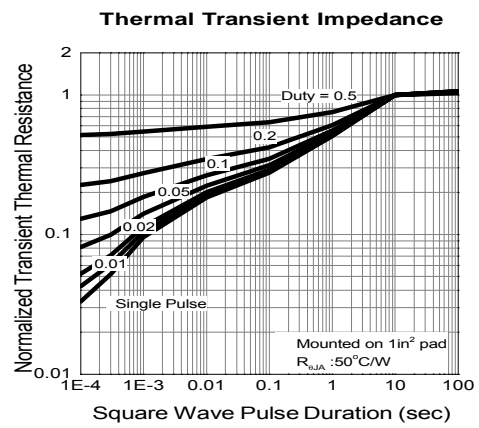
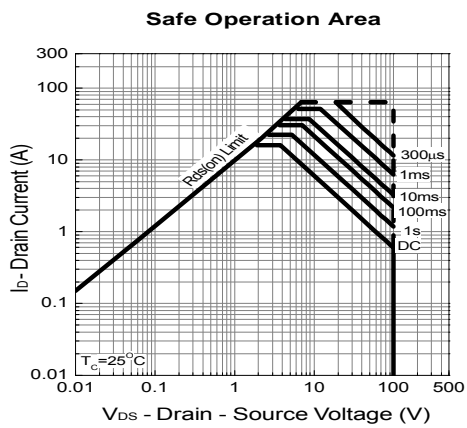
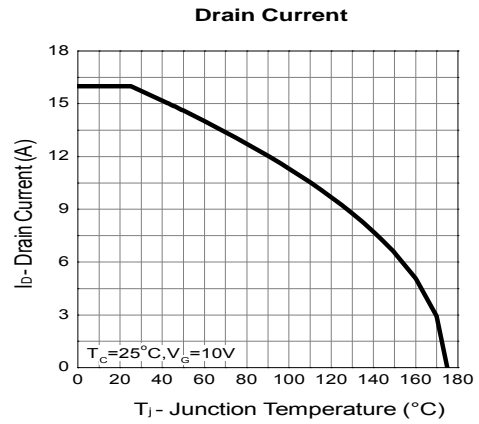
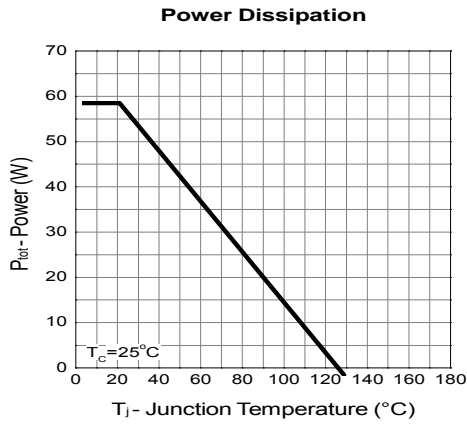
Symbol	Parameter	Test Conditions	15N10			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=80V, V_{GS}=0V$	-	-	1	μA
		$T_J=85^\circ\text{C}$	-	-	30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1.5	2	2.5	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 16V, V_{DS}=0V$	-	-	± 10	μA
$R_{DS(ON)}^a$	Drain-Source On-state Resistance	$V_{GS}=10V, I_{DS}=15A$	-	80	100	m Ω
		$V_{GS}=4.5V, I_{DS}=8A$	-	115	130	
Diode Characteristics						
V_{SD}^a	Diode Forward Voltage	$I_{SD}=5A, V_{GS}=0V$	0.6	0.8	1.1	V
t_{rr}	Reverse Recovery Time	$I_{DS}=5A, di_{SD}/dt=100A/\mu s$	33	47	61	ns
Q_{rr}	Reverse Recovery Charge		61	87	113	nC
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=30V,$ Frequency=1.0MHz	730	940	1250	pF
C_{oss}	Output Capacitance		45	80	115	
C_{rss}	Reverse Transfer Capacitance		25	50	75	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=30V, R_L=30\Omega,$ $I_{DS}=1A, V_{GEN}=10V,$ $R_G=6\Omega$	-	13	24	ns
t_r	Turn-on Rise Time		-	10	19	
$t_{d(OFF)}$	Turn-off Delay Time		-	32	60	
t_f	Turn-off Fall Time		-	16	30	
Gate Charge Characteristics ^b						
Q_g	Total Gate Charge	$V_{DS}=50V, V_{GS}=10V,$ $I_{DS}=5A$	12	21	30	nC
Q_{gs}	Gate-Source Charge		3.4	4.9	6.4	
Q_{gd}	Gate-Drain Charge		2.9	5.8	8.7	

Note a : Pulse test ; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

Note b : Guaranteed by design, not subject to production testing.

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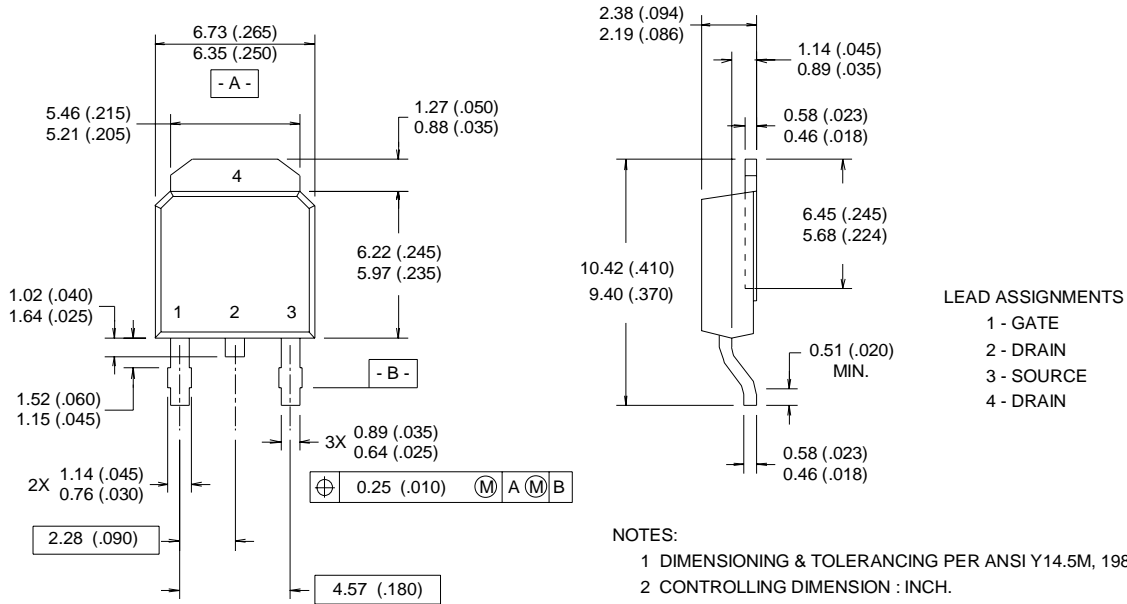
■ TYPICAL CHARACTERISTICS (25°C Unless Note)



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TO-252 Outline Package Dimension

Dimensions are shown in millimeters (inches)



PACKAGE OUTLINE SOP-8P

