Description

The BM0458 synchrnous buck onverter is designed to regulate over a wide input voltage range, minimizing the need for external surge suppression components. A minimum controllable on-time of 150ns facilitates large step-down conversion ratios, enabling the direct step-down from a 48V nominal input to low-voltage rails for reduced system complexity and solution cost.

The BM0458 operates during input voltage dips as low as 6.5V, at nearly 100% duty cycle if needed, making the device an excellent choice for wide input supply range industrial and high cell count battery pack applications.

With integrated high-side and low-side power MOSFETs, the BM0458 delivers up to 1A of output current. A constant on-time (COT) control architecture provides nearly constant switching frequency with excellent load and line transient response.

The BM0458 is available in ESOP-8package.

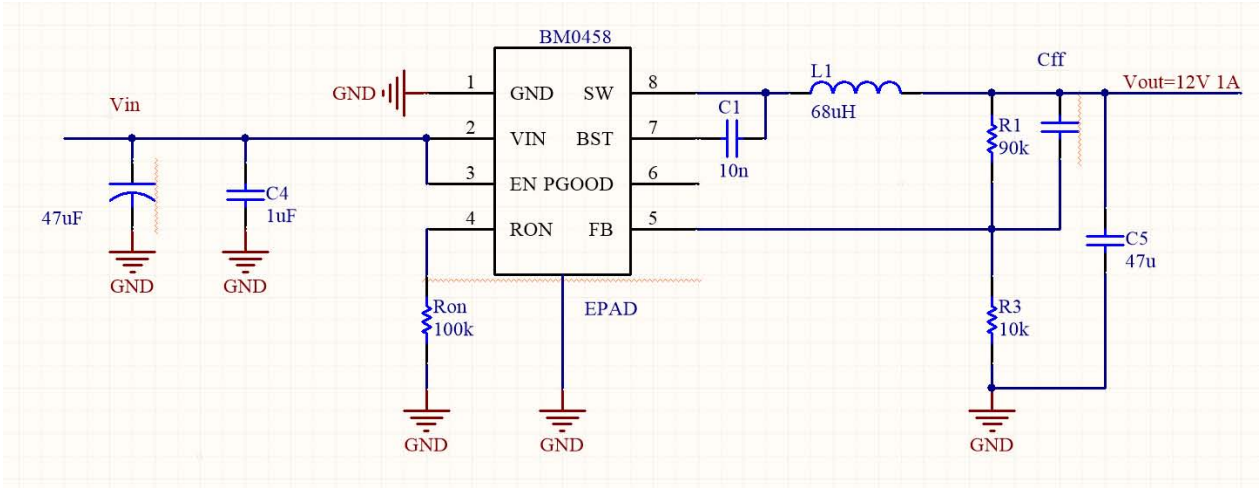
Features

- Designed for reliable and rugged applications
- Wide input voltage range of 6.5V to 100V
- Junction temperature range: –40°C to +160°C
- Fixed 3ms internal soft-start timer
- Input UVLO and thermal shutdown protection
- Low minimum on- and off-times of 150ns
- Adjustable switching frequency up to 1MHz
- Diode emulation for high light-load efficiency
- 11μA no-load input quiescent current
- 4μA shutdown quiescent current
- COT mode control architecture
- No loop compensation components
- Internal VCC bias regulator and boot diode
- Open-drain power good indicator
- ESOP-8 package

Applications

- E-bike/ E-scooter
- Motor Drives
- Industrial Equipment
- Energy Storage System

Typical Application



当输出电流超过0.5A时，输出对地多并一个100uF电解电容

Absolute Maximum Ratings (at TA = 25°C)(1)

		MIN	MAX	UNIT
Input Voltage	VIN to GND	-0.3	110	V
	EN to GND	-0.3	110	
	FB to GND	-0.3	6.5	
	RON to GND	-0.3	6.5	
Bootstrap Capacitor	External BST to SW capacitance	4.7	22	nF
Output Voltage	BST to GND	-0.3	SW+6.5V	V
	BST to SW	-0.3	6.5	
	SW to GND	-1.5	110	
	SW to GND(20 ns transient)	-3		
	PGOOD to GND	-0.3	33	
T_J	Junction temperature	-40	160	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
	Charger device model (CDM)	±1000	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

超低静态电流<15uA，同步整流，内置PMOS　近100%占空比 ；
超低输入输出压差，低启动电压　频率可外部设置 ；
平替LM5163与5164 也可替MK9019　功能替代MP4580

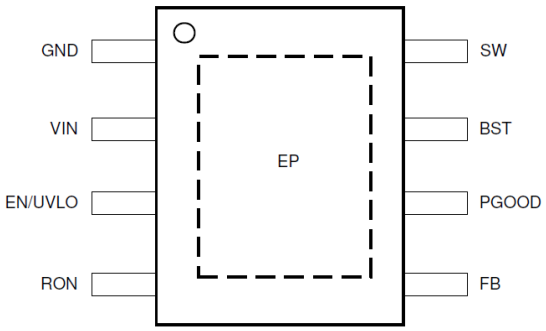
Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	6.5		100	V
V_{SW}	Switching node voltage			100	V
V_{EN}/UVLO	Enable voltage			100	V
I_{LOAD}	Load current		1		A
Frequency	Switching frequency	100		1000	KHz
C_{BST}	External BST to SW capacitance		10		nF
T_{ON}	Programmable on time	50		10000	ns

Order Information

Product Name	Part Number	Package	SPQ
BM0458	BM0458	ESOP-8	4000

Pin Function and Descriptions



Package ESOP-8 Top View

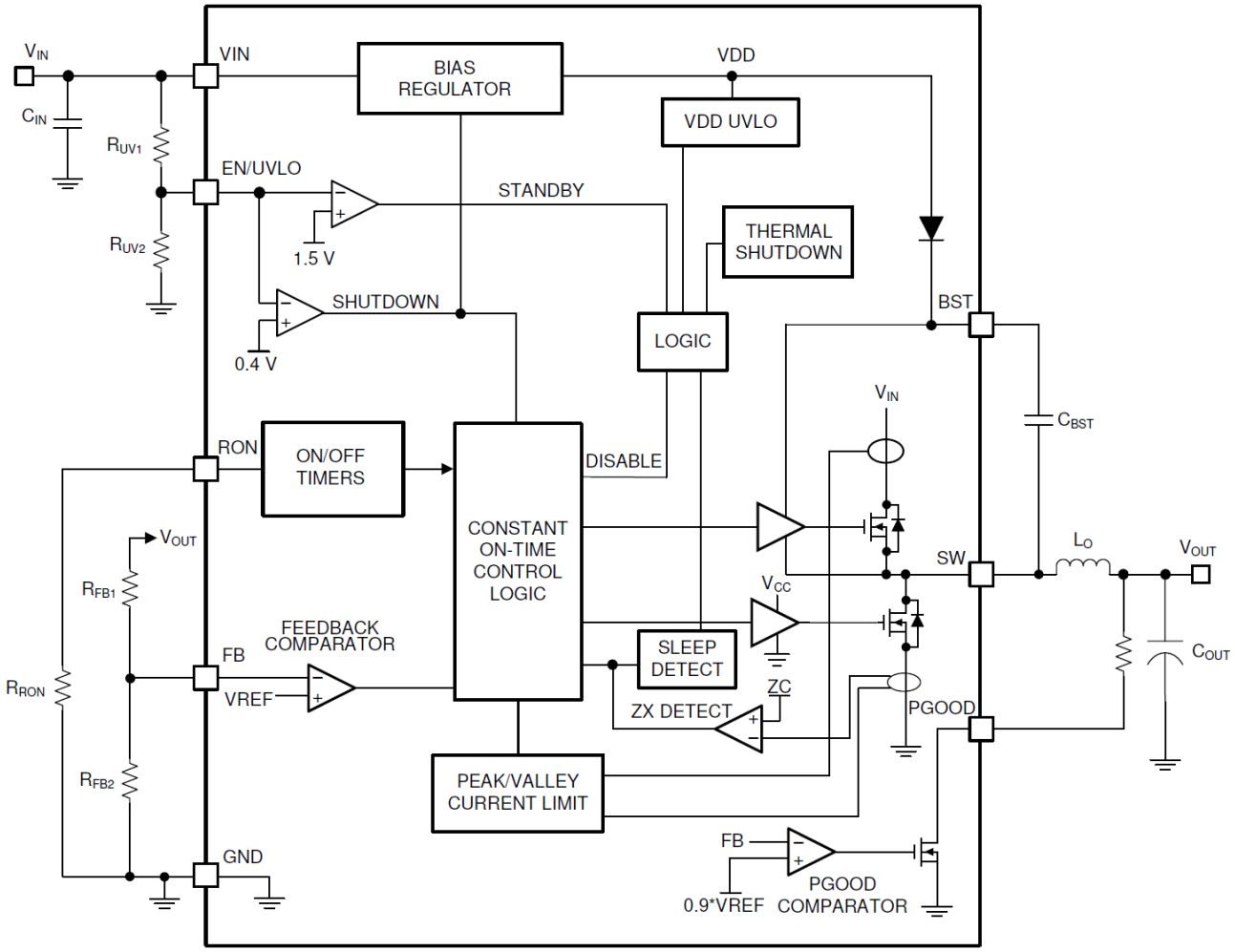
Pin		Type	Description
NO.	Name		
1	GND	G	Ground connection for internal circuits
2	VIN	P/I	Regulator power input pin
3	EN/UVLO	I	Enable and UVLO programing pin
4	RON	I	On-time programing pin. A resistor between this pin and GND sets the buck switch on-time.
5	FB	I	Feedback input of voltage regulation comparator
6	PGOOD	O	Power good indicator, open-drain output pin. Connect to a source voltage through an external pullup resistor between 10 kΩ to 200 kΩ.
7	BST	P/I	Bootstrap gate-drive supply. Required to connect a high-quality 10 nF 50 V X7R ceramic capacitor between BST and SW to bias the internal high-side gate driver.
8	SW	P	Switching node. Connect to the switching node of the power inductor.
-	EP	-	Exposed pad of package. Solder the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.

Electrical Characteristics

Typical values correspond to TJ = 25° C. Minimum and maximum limits apply over the full －40° C to 150° C junction temperature range unless otherwise indicated. VIN = 48 V and VEN/UVLO = 2 V unless otherwise stated.

PARAMETER		TEST CONDITION	MIN	TYPE	MAX	UNIT
SUPPLY CURRENT						
$I_{Q-SHUTDOWN}$	VIN shutdown current	V_{EN} = 0V		4		uA
$I_{Q-SLEEP}$	VIN sleep current	V_{EN}=2.5V, VFB=1.5V		11		uA
$I_{Q-ACTIVE}$	VIN active current	V_{EN}=2.5V, No load		16.2		uA
EN/UVLO						
$V_{SD-RISING}$	Shutdown threshold	$V_{EN/UVLO}$ rising			1.1	V
$V_{SD-FALLING}$	Shutdown threshold	$V_{EN/UVLO}$ falling	0.45			V
$V_{EN-RISING}$	EN threshold	$V_{EN/UVLO}$ rising		1.5		V
$V_{EN-FALLING}$	EN threshold	$V_{EN/UVLO}$ falling		1.4		V
FEEDBACK						
V_{REF}	FB regulation voltage	V_{FB} falling	1.18	1.2	1.22	V
TIMING						
T_{ON1}	On-time 1	VIN=6V, RON=75KΩ		4400		ns
T_{ON2}	On-time 2	VIN=6V, RON=25KΩ		1600		ns
T_{ON3}	On-time 3	VIN=12V, RON=75KΩ		2200		ns
T_{ON4}	On-time 4	VIN=12V, RON=25KΩ		1000		ns
PGOOD						
V_{PG-UTH}	FB upper threshold for PGOOD high to low	V_{FB} rising		1.1		V
V_{PG-LTH}	FB lower threshold for PGOOD low to high	V_{FB} falling		1.03		V
V_{PG-HYS}	PGOOD threshold hysteresis	V_{FB} falling		70		mV
R_{PG}	PGOOD pull down resistance	V_{FB} = 1V		50		Ω
BOOTSTRAP						
V_{BST-UV}	Gate drive UVLO	V_{BST} rising		2.7		V
POWER SWITCHES						
$R_{DSON-HS}$	High side MOS R_{DSON}	I_{SW} = -100mA		0.75		Ω
$R_{DSON-LS}$	Low side MOS R_{DSON}	I_{SW} = 100mA		0.35		Ω
SOFT START						
T_{SS}	Soft start time			3		ms
CURRENT LIMIT						
I_{peak}	Peak current limit			1.4		A
I_{valley}	Valley current limit			1		A

Functional Block Diagram



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Feature Description

Control Architecture

The BM0458 step-down switching converter emply by a constant on-time (COT) control scheme. The COT control scheme sets a fixed on-time T_{ON} of the high-side FET using a timing resistor (R_{ON}). The T_{ON} is adjusted as Vin changes and is inversely proportional to the input voltage to maintain a fixed frequency when in continuous conduction mode (CCM). After expiration of T_{ON}, the high-side FET remains off until the feedback pin is equal or below the reference voltage of 1.2 V. To maintain stability, the feedback comparator requires a minimal ripple voltage that is in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage during the off-time must be large enough to dominate any noise present at the feedback node. The minimum recommended ripple voltage is 20 mV.

During a rapid start-up or a positive load step, the regulator operates with minimum off-times until regulation is achieved. This feature enables extremely fast load transient response with minimum output voltage undershoot. When regulating the output in steady-state operation, the off-time automatically adjusts itself to produce the SW-pin duty cycle required for output voltage regulation to maintain a fixed switching frequency. In CCM, the switching frequency F_{SW} is programmed by the R_{RON} resistor. Use Equation 1 to calculate the switching frequency.

$$F_{SW}(KHz) = V_{OUT}(V) \times 2500/R_{RON}(K\Omega) \quad (1)$$

Diode emulation mode (DEM) prevents negative inductor current, and pulse skipping maintains the highest efficiency at light load currents by decreasing the effective switching frequency. DEM operation occurs when the synchronous power MOSFET switches off. Here, the load current is less than half of the peak-to-peak inductor current ripple in CCM. Turning off the low-side MOSFET at zero current reduces switching loss, and preventing negative current conduction reduces conduction loss. Power conversion efficiency is higher in a DEM converter than an equivalent forced-PWM CCM converter. With DEM operation, the duration that both power MOSFETs remain off progressively increases as load current decreases. When this idle duration exceeds 15 us, the converter transitions into an ultra-low I_Q mode, consuming only 11 uA quiescent current from the input.

Device Functional Modes

-Shutdown Mode

EN/UVLO provides ON and OFF control for the BM0458. When V_{EN} UVLO is below approximately 1.1 V, the device is in shutdown mode. Both the internal linear regulator and the switching regulator are off. The quiescent current in shutdown mode drops to 4 uA at VIN = 24 V. The BM0458 also employs internal bias rail undervoltage protection. If the internal bias supply voltage is below the UV threshold, the regulator remains off.

-Active Mode

The BM0458 is in active mode when Ven UVLO is above the precision enable threshold and the internal bias rail is above its UV threshold. In COT active mode, the BM0458 is in one of three modes depending on the load current:

1. CCM with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple;
2. Pulse skipping and diode emulation mode (DEM) when the load current is less than half of the peak-to-peak inductor current ripple in CCM operation;
3. Current limit CCM with peak current limit protection when an overcurrent condition is applied at the output.

-Sleep Mode

The converter enters DEM during light-load conditions when the inductor current decays to zero and the synchronous MOSFET is turned off to prevent negative current in the system. In the DEM state, the load current is lower than half of the peak-to-peak inductor current ripple and the switching frequency decreases when the load is further decreased as the device operates in a pulse skipping mode. A switching pulse is set when V_{FB} drops below 1.2 V.

As the frequency of operation decreases and V_{FB} remains above 1.2 V (V_{REF}), the converter enters an ultra-low I_Q sleep mode to prevent draining the input power supply. The input quiescent current (I_Q) required by the BM0458 decreases to 11 uA in sleep mode , improving the light-load efficiency of the regulator.

Internal VCC Regulator and Bootstrap Capacitor

The BM0458 contains an internal linear regulator that is powered from V_{IN} with a nomina ouput of 5V, eliminating the need for an external capacitor to stabilize the linear regulator. As the power MOSFET has a low total gate charge, use a low bootstrap capacitor value to reduce the stress on the internal regulator. It is required to select a high-quality 10nF 50V X7R ceramic bootstrap capacitor. Selecting a higher value capacitance stresses the internal VCC regulator and damages the device. A lower capacitance than required is not sufficient to drive the internal gate of the power MOSFET.

Regulation Comparator

The feedback voltage at FB is compared to an internal 1.2V reference. The BM0458 voltage regulation loop regulates the output voltage by maintaining the FB voltage equal to the internal reference voltage, V_{REF}. A resistor divider programs the ratio from output voltage V_{OUT} to FB. For a target V_{OUT} setpoint, use Equation 2 to calculate R_{FB2} based on the selected R_{FB1}.

$$\mathbf{R_{FB2} = 1.2V \times R_{FB1}/(V_{OUT} - 1.2V)} \qquad \mathbf{(2)}$$

Selecting R_{FB1} in the range of 100 kΩ to 1 MΩ is recommended for most applications. A larger R_{FB1} consumes less DC current, which is mandatory if light-load efficiency is critical. R_{FB1} larger than 1 MΩ is not recommended as the feedback path becomes more susceptible to noise. It is important to route the feedback trace away from the noisy area of the PCB and keep the feedback resistors close to FB pin.

On-Time Generator

The on-time of the BM0458 high-side FET is determined by the R_{RON} resitor and is inversely proportional to the input voltage V_{IN}. The inverse relationship with V_{IN} results in a nearly constant frequency as V_{IN} is varied. Use Equation 3 to calculate the on-time.

$$\mathbf{T_{ON}(us) = R_{RON}(K\Omega)/(V_{IN}(V) \times 2.5)} \qquad \mathbf{(3)}$$

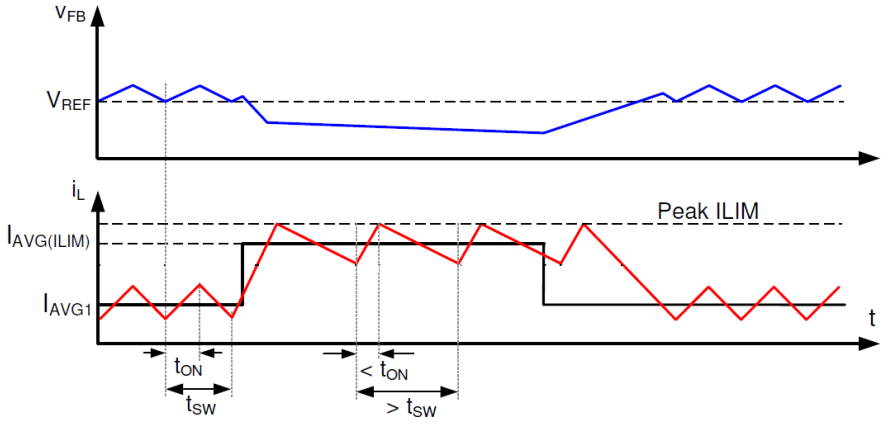
Use Equation 4 to determine the R_{RON} resistor to set a specific switching frequency in CCM.

$$R_{RON}(K\Omega) = V_{OUT}(V) \times 2500/F_{SW}(KHz) \qquad (4)$$

Select R_{RON} for a minimum on-time (at maximum V_{IN}) greater than 50 ns for proper operation. In addition to this minimum on-time, the maximum frequency for this device is limited to 1 MHz.

Current Limit

The BM0458 manages overcurrent conditions with cycle-by-cycle current limiting of the peak and valley inductor current. The current sensed in the high-side MOSFET is compared every switching cycle to the current limit threshold. As shown in Figure below, if the peak current in the high-side MOSFET exceeds 1.5 A (typical), the present cycle is immediately terminated regardless of the programmed on-time (T_{ON}), the high-side MOSFET is turned off ， the low-side MOSFET remains on, after which the next on-pulse is initiated. This method folds back the switching frequency to prevent overheating and limits the average output current to less than 1A to ensure proper short-circuit and heavy-load protection of the BM0458.



Enable/Undervoltage Lockout (EN/UVLO)

The BM0458 contains a dual-level EN/UVLO circuit. When the EN/UVLO voltage is below 1.1 V (typical), the converter is in a low-current shutdown mode and the input quiescent current (I_Q) is dropped down to 4 uA. When the voltage is greater than 1.1 V but less than 1.5 V (typical), the converter is in standby mode.

Power Good (PGOOD)

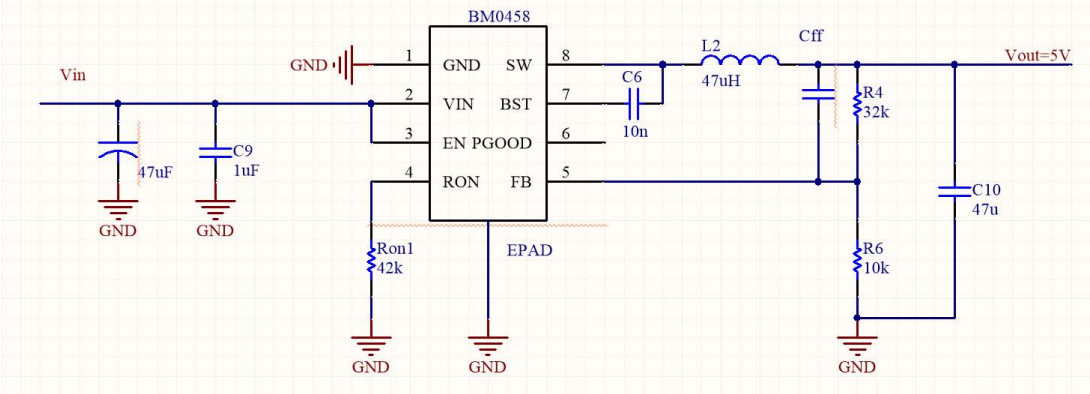
The BM0458 provides a PGOOD flag pin to indicate when the output voltage is within the regulation level Use the PGOOD signal for start-up sequencing of downstream converters or for fault protection and output monitoring. PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 33 V. The typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail. When the FB voltage exceeds 95% of the internal reference VREF, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pullup. If the FB voltage falls below 90% of V_{REF}, an internal 50Ω PGOOD switch turns on and PGOOD is pulled low to indicate that the output voltage is out of regulation. The rising edge of PGOOD has a built-in deglitch delay of 5 us.

Thermal Protection

The BM0458 includes an internal junction temperature monitor to protect the device in the event of a higher than normal junction temperature. If the junction temperature exceeds 165° C (typical), thermal shutdown occurs to prevent further power dissipation and temperature rise. The BM0458 initiates a restart sequence when the junction temperature falls to 155° C, based on a typical thermal shutdown hysteresis of 10° C. This is a non-latching protection, so the device cycles into and out of thermal shutdown if the fault persists.

Application Information

Typical Application



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Recommended External Components for Application

V_{OUT} (V)	R_{ON} (K Ω)	Frequency (MHz)	L_{OUT} (uH)
5	25	0.5	22
	40	0.3	47
	125	0.1	100
12	60	0.5	47
	100	0.3	68
	300	0.1	150
30	150	0.5	68
	250	0.3	68
	750	0.1	330

Input Capacitor (C_{IN})

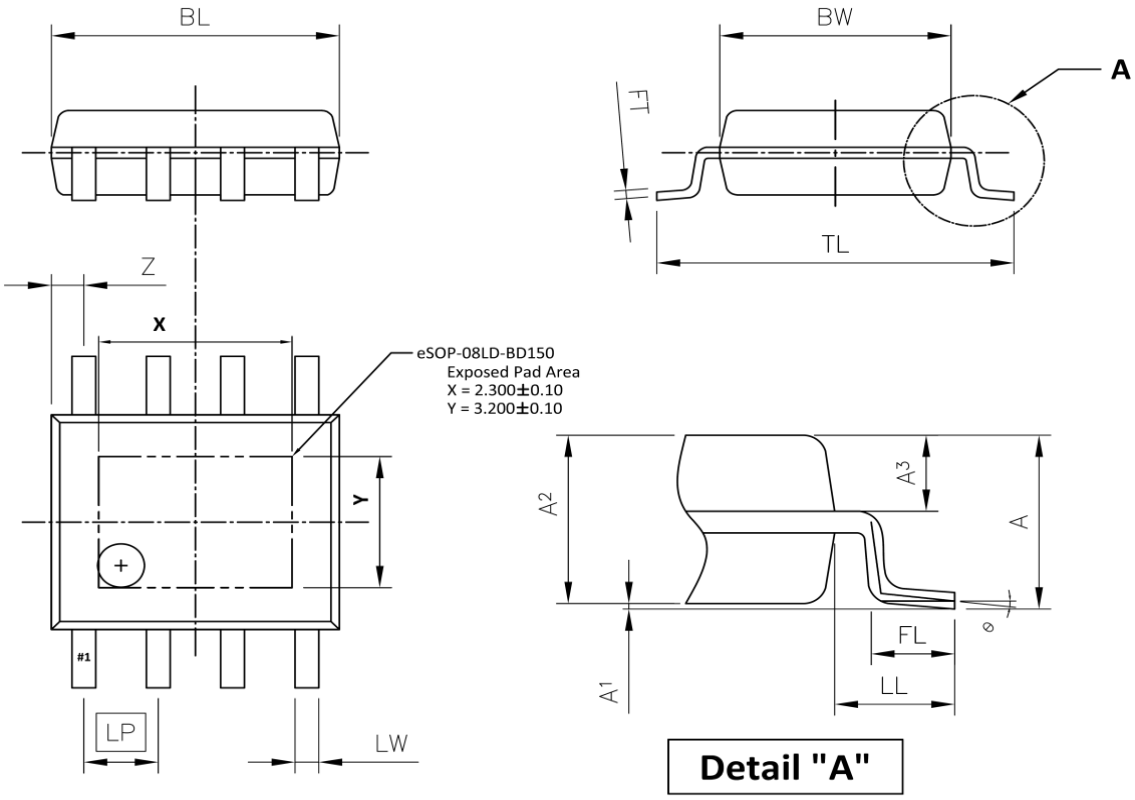
An input capacitor is necessary to limit the input ripple voltage while providing AC current to the buck power stage at every switching cycle. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the V_{IN} and GND pins of the BM0458.The recommended high-frequency input capacitance is 2.2 uF or higher. Ensure the input capacitor is a high quality X7S or X7R ceramic capacitor with sufficient voltage rating for C_{IN}.

Output Capacitor (C_{OUT})

Select a ceramic output capacitor to limit the capacitive voltage ripple at the converter output. This is the sinusoidal ripple voltage that is generated from the triangular inductor current ripple flowing into and out of the capacitor. With voltage coefficients of ceramic capacitors taken in consideration, a 22uF or higher as 47uF capacitor with X7R dielectric is selected.

Package Outline Dimensions

ESOP-8



Symbol	Dimensions in Millimeters		
	Min.	Nom.	Min.
BL	4.74	4.92	5.10
BW	3.75	3.95	4.15
FT	0.195	0.203	0.211
TL	6.00	6.10	6.20
LP	1.245	1.270	1.295
LW	0.375	0.400	0.425
A	-	-	1.75
A1	0.05	-	0.25
A2	1.50	-	1.60
A3	0.675(BSC)		
LL	1.05(BSC)		
FL	0.50	-	0.80
X	2.200	2.300	2.400
Y	3.100	3.200	3.300
Z	-	0.55	-
θ	0°	-	8°